New Technologies for Contactless Microsystems

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Abstract

This paper presents some new emerging technological avenues for contactless chips in order to tackle emerging and demanding future specifications. Basically RFID chips will evolve towards new embedded functions such as power, sensing and security.

Today, R&D works on future contactless Microsystems can be clustered into four main directions:

- Silicon technologies for low power and non volatile memories
- Contactless air interfaces
- Embedded micro power sources
- Embedded micro-sensors

1. Introduction

The current and basic architecture of a RFID chip is shown in figure 1. It has three main functions: First, the RX/TX bloc which runs communication and energizing through the electromagnetic field emitted by the reader. Second, the digital sequencer which decodes and executes the messages sent by the reader. Third, the non volatile memory which stores data, at least the ID code.

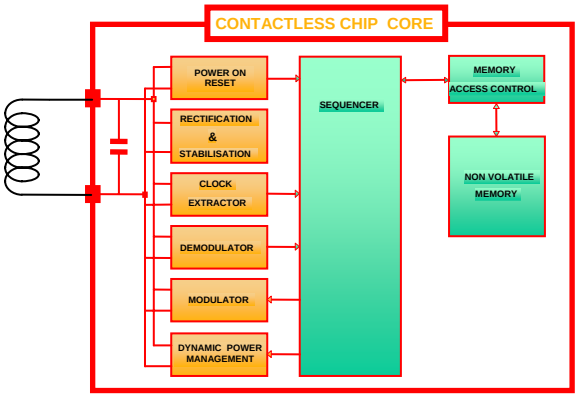


Fig. 1: Basic architecture of RFID chip

To improve the low power performances of basic RFID chips technological changes have to be done at the silicon process level. SOI technology appears to be a good candidate. Contactless air interface can be improved at different points: antennas, higher data rates, longer range and multi-tag protocols.
Moreover new embedded functions may be added to the chip to increase its profitability. Micro-sensors with data acquisition and power sources can extend raw identification to data logging for enhanced traceability of goods. Figure 2 shows the architecture with new functions.

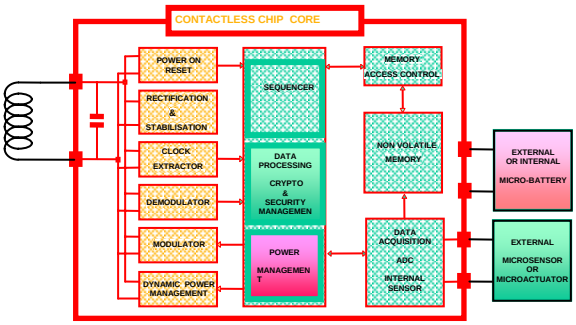


Fig. 2: RFID chip architecture with sensing

2. Low voltage/low power technologies

SOI technology offers several key characteristics for RFID chips. The high resistivity of the substrate reduces the associated current leakage and so the required power. This provides also a better isolation between RF RX/TX bloc and digital sequencer. Which is very important for mixed type chips such as RFID ones. Figure 4 shows a prototype of a RFID chip designed in 0.25 µm.

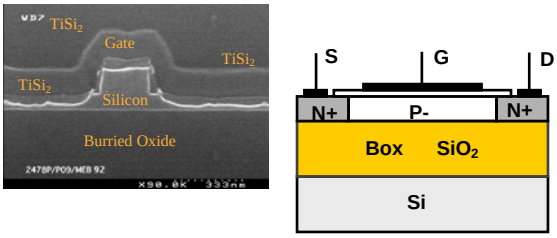


Fig. 3: SOI process and basic transistor

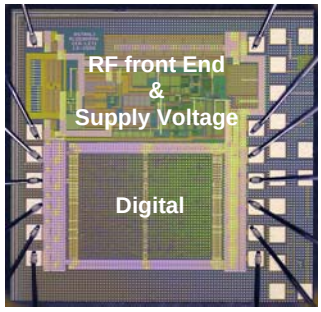
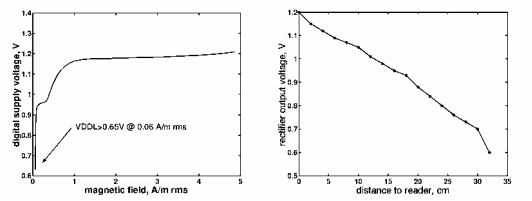


Fig. 4: RFID chip in 0.25µm SOI



(5) (6)

Fig.5:Digital supply voltage vs field intensity
Fig.6: Tag rectifier output voltage vs distance to reader

The power and clock recovery functionality is illustrated on figure 6 where the rectifier output voltage is plotted versus the distance to a 0.6 W reader with a 13 cm diameter antenna at a frequency carrier of 13.56MHz. The maximum distance allowing a correct clock recovery is 32 cm. This is a good result that can be compared to the 22 cm limit obtained with a reference 0.6 µm bulk CMOS chip. It is worth noticing that the minimum supply voltage of the clock recovery block is very close to the DC threshold voltage absolute value of N and P type transistors. This occurs thanks to the well-known dynamic threshold voltage effect and proves that the use of SOI has a significant part in performance improvement.
The digital block proved functional for a supply voltage ranging from 1.8 V down to 0.6 V which is a very interesting feature for future developments. See figure 5 for the digital supply voltage versus distance to reader.

3. New Non Volatile Memory

The current non volatile memory technology for embedded memory relies on EEPROM and Flash (Page Flash). The main drawbacks for contactless chips are: too long writing time (few ms) and high voltage for bit cells programming with power demanding charge pumps. Sensitivity to IR radiations erasure is of concern for security aspects.

Several new technologies are under investigation: M-Ram, Fe-Ram, PC-Ram, organic memory and MEMS.
The very recent and innovative MEMS approach relies on micro mechanical bistable switches. No power is required in retention mode. The micro-mechanic assembly is resistant to EM radiations. The drawback is the cells density. But 128 bits is low anyway. One Time Programmable (OTP) and Multi-Time programmable (MTP) arrays of bits may be achieved. Writing energy is as low as 25 pJ/bit, writing is few µs. This non-volatile memory cells retains their programmed state irrespective of supply voltage or extremes of mechanical shock temperature or radiation.

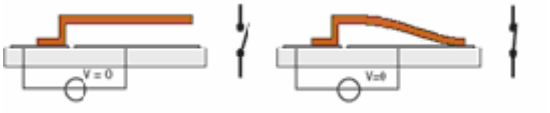


Fig. 7: Two stable states micro-cantilever

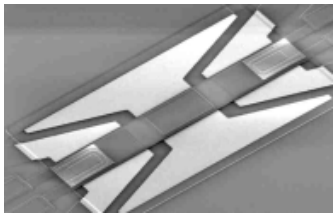


Fig. 8: Example of micro mechanical switch

Anothere promising emerging technology is PC-Ram. It uses a biphase material (chalcogenide). One state is amorphous with high resistivity, the second is crystalline with low resistivity. The power required to write a word is very low and write time is fast and close to read time (few 10ns). With these performances and RFID requirements, unified memory mapping is so achievable: only one technology in place of registers, RAM, ROM, EEPROM.

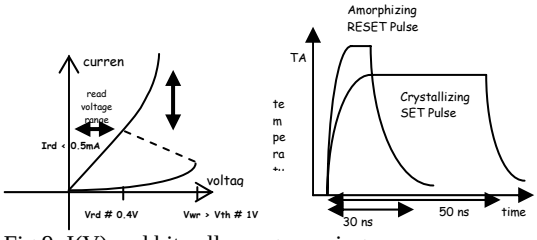


Fig 9: I(V) and bit cells programming curves

4. Very High Data Rates for Contactless Interface

The contactless smart card market is quickly evolving towards new applications and new services. These new smart secure portable objects will need higher contactless data rates for files, images and databases transfers. New modulation/coding schemes are mandatory to provide up to several Mbps links. A first work has been done to break the 1 Mbps barrier.

Reader to card: In order to break the 1 Mbps barrier some care must be taken to fit radio emission regulation and power transfer efficiency. Because bandwidth is limited by quality factors of antennas, the solution investigated is to increase the number of bits per transmitted symbols. Because the signal to noise ratio is quite fair for proximity coupling, and by continuity with the standard ISO 14443 type B, the modulation from reader to card is multilevel amplitude modulation.

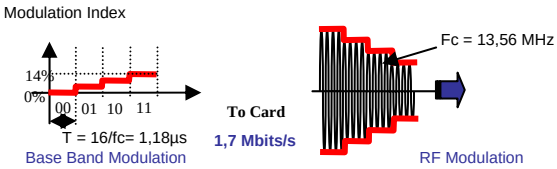


Fig 10: Multi levels amplitude modulation

	2 levels : 2^1	4 levels : 2^2	8 levels : 2^3	16 levels : 2^4
T = 128 /fc (9,4 µs)	106 kbits/s	212 kbits/s	318 kbits/s	424 kbits/s
T = 64 /fc (4,72 µs)	212 kbits/s	424 kbits/s	636 kbits/s	848 kbits/s
T = 32 /fc (2,36 µs)	424 kbits/s	848 kbits/s	1271 kbits/s	1695 kbits/s
T = 16 /fc (1,18 µs)	848 kbits/s	1695 kbits/s	2542 kbits/s	3390 kbits/s

Table 1: Reader to card bits rates

A dynamic correction to compensate amplitude variations generated from relative movement of the card is implemented. A specific start of frame (SOF) is used in the header of a data bloc, which adapt continuously the range of the amplitude variation for the receiver.

Card to reader: The return channel from card to reader is multi phase modulation on sub carrier.

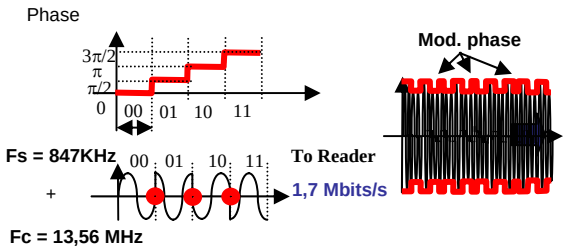


Fig 11: Multi phases on sub-carrier modulation

	2 ϕ □: 2^1 180 °	4 ϕ : 2^2 (90°)	8 ϕ : 2^3 (45°)	16 ϕ □: 2^4(23°)
fs = 848 kHz				
T =2Ts (2,36 µs)	**424 kbits/s**	**848 kbits/s**	**1271 kbits/s**	**1695 kbits/s**
T = Ts (1,18 µs)	**848 kbits/s**	**1695 kbits/s**	**2543 kbits/s**	**3390 kbits/s**
fs = 1,7 MHz				
T = 2Ts (1,18 µs)	**848 kbits/s**	**1695 kbits/s**	**2542 kbits/s**	**3390 kbits/s**
T = 1Ts (0,59 µs)	**1695 kbits/s**	**3390 kbits/s**	**5085 kbits/s**	**6780 kbits/s**

Table 2: Card to reader bit rates

The data link was successfully tested at a data rate of 1.7 Mbps with a 5 cm distance between the reader and the card, 4 levels of amplitude, a symbol time of 1.18µs from reader to card and either 4 phases on a sub carrier at 848 kHz or 2 phases on a sub carrier at 1.7 MHz from card to reader In a magnetic field of 2.3A/m, the measured Bit Error Rate is to 10^{-7} for the reader to card link and to 10^{-9} for the card to reader link. Higher data rates are currently under validation.

5. Asynchronous air interface

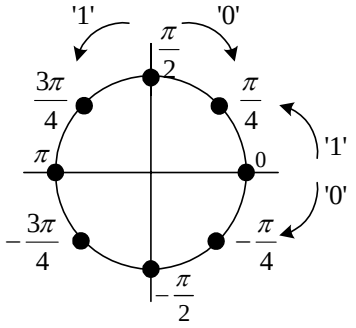
The innovative tag front-end presented in this section enables asynchronous transmissions from reader to tag, with a 13.56 MHz frequency carrier. To achieve this, an event based communication is designed to send information at any data rate up to system limitations. A dynamically adaptation to environment conditions is now possible controlling data transmission rate.

The local synchronization distributes block activations over time. Those two properties may reduce static and dynamic power consumption. The delay insensitive property of those circuits makes them robust to supply voltage variations: a computing speed regulation, depending on available power supply on tag, is automatically implemented. This also reduces tag front-end constraints and consequently its complexity and area.

The goal of this event based communications is to replace classical transmissions, based on fixed and predefined data transmission rates, by variable data rate transmissions. Data clock edges are replaced by asynchronous events. To detect such communications, the tag has to implement an asynchronous event detector to synchronise the demodulation with data sent by the reader. As the tag does not have to generate a data clock, there is no time constraint for the tag design: it is able to work at any data transmission rate up to a maximum data rate depending of the process and design.

The reader to tag asynchronous communication is implemented using a phase modulation and an original code called CAC, for Cyclic Asynchronous Code, with 8 states. Height states is a right tradeoff for reducing the amplitude drop in the envelop of the carrier without jeopardizing the power transfer. At any moment, two choices for the next state, on eight available, are possible to code the two logical values. The code is illustrated in the next figure. Tag to reader communication is implemented using a CAC with 4 states code. See figure 12 for the modulation/coding scheme.

An asynchronous communication from the reader to the tag is shown below. First, data and synchronization sent to the modulator are given. The phase position of the carrier, selected according to the encoding scheme, is then presented. Finally, the signal received on tag coil is given, showing that each phase shift produces an amplitude variation of this signal, with a modulation index below 6%, due to the filtering function of the inductive link.



$$|\varphi_{n+1} - \varphi_n| = \frac{\pi}{4}$$

Fig 12: The modulation/coding scheme

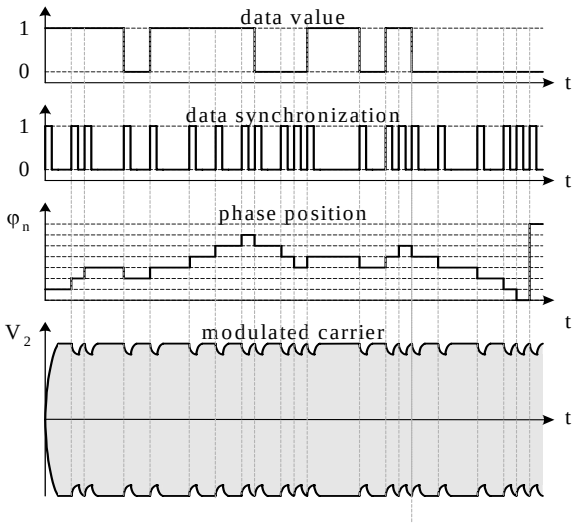


Fig 13: Chronograms

The presented architecture has been implemented on a 6 metal-layer, 130 nm and 1.2 V supply voltage standard CMOS process from ST Microelectronics. The area of the test chip is 1.38 mm^2, including test pads and a 600 pF decoupling capacitor.

Communication distance (cm)	0	10	15
Supply voltage V_{CCA} (V)	1.18	0.94	0.90
Power consumption (µW)	116	74.7	68.9
Maximum data rate (Mbps)	1.0	1.2	1.0

Table 3: Asynchronous RX performances

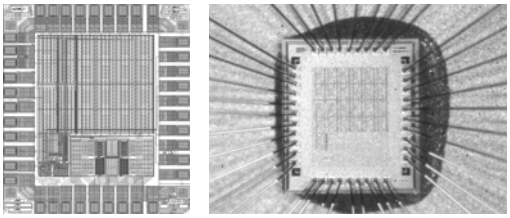


Fig 14: Test chip

Asynchronous communications have been tested up to a maximum data rate according tag position in the magnetic field. The table upper gives tag front end power consumption and maximum data rate allowed by the system according to communication distances. With a power consumption below 120 µW, an asynchronous reader to tag transmission up to 1.2 Mbps is possible.

6. Micro-Antennas

Back-end upper layer has been added to integrate micro-coils embedded on the chip. The purpose is to reduce fabrication costs for application where the reading distance is some few millimetres, using profitability of collective manufacturing on silicon wafers. To get correct quality factor for the BF antenna (#20) thin copper (10µm) etching and deposit has been developed. Results are quite promising because a Q factor of 30 with a coil of 25 turns was validated on a 4x4 mm^2 die representative of a smart card chip.

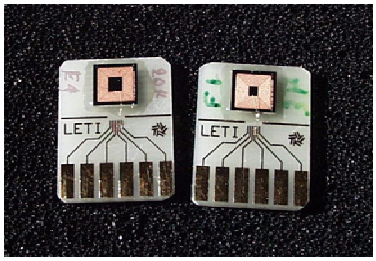


Fig. 15: Coils on chip in thin copper

7. Micro power sources

Because passive tags cannot handle data acquisition when far from the electromagnetic field of a reader, a power source is required to supply the data acquisition functions: sensors, analogue to digital converters and non volatile memory storage.
Two types of miniaturised power sources are under development: a thin film battery and a micro-battery.
Thin film battery is dedicated to provide the main energy. It is layered onto the substrate of the tag. Several tens of mA.h can be available from a 5 cm^2 by 400 µm of thickness power source.
The main qualities are:

- Flexible for Tags or Smart Cards
- Fast recharge < 3mn for 20mA.h under 2V
- Roll to roll process :
  - Ink elaboration by mixing
  - Coating and drying
  - Calandering
  - Assembling
  - Electrolyte filling and packaging

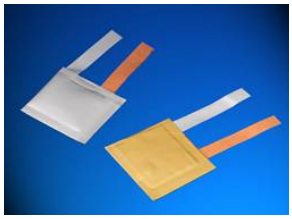


Fig. 16: Thin film flexible batteries

Micro-battery is a miniaturized power source which can be embedded onto the chip. The process is quite similar to “Above IC” process. Five extra layers are necessary to manufacture the micro-battery: current collector, cathode, electrolyte, anode and packaging. The electrolyte is a solid state one, which is very compatible with solid state semiconductor manufacturing. So, the whole process is compatible with semiconductor assembly lines. The total thickness is 10µm and available energy is 100 to 200 µA.h per cm^2. The total thickness with packaging is 15 µm. Available voltages are in the 1.6 to 2.8 range. Because the surface of the micro-battery is any geometrical form the maximum power can be embedded onto the chip. Last but not least, associated mask set is very cheap because no very high precision is required.

This energy enables to have a Real-Time-clock (RTC) module fully autonomous inside the chip. This allows to time stamp data and events that are recorded into the non volatile memory.

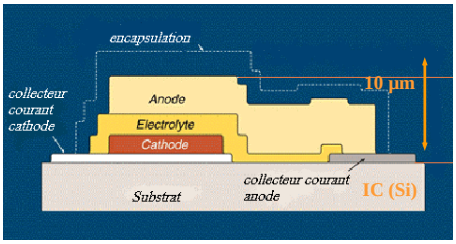


Fig. 17: Micro-battery in “Above IC” technology

8. Micro-sensors

Many micro-sensors have been developed in the past few years. Most time power requirements are low, so it is possible to associate them to electronic tags and to use the same contactless interface to download the registered data. Traceablity of physical parameters between two reader connections is enabled if micro power sources are also integrated. Most time these micro-sensors are manufactured with a specific technology because of manufacturing process or high resolution requirements. So a multi chip module technique will be mandatory to electronic tags with sensing capabilities. Micro-packaging will be a key point.

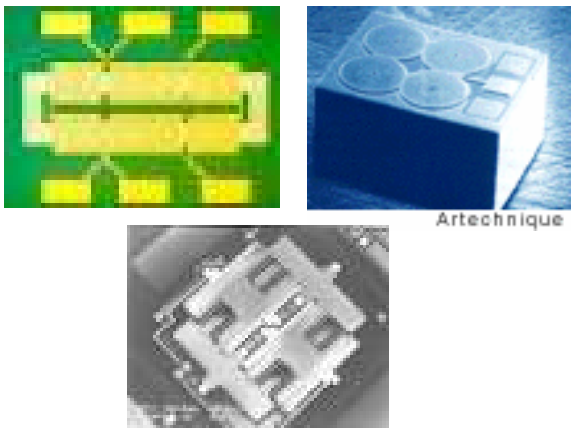


Fig. 18: magnetometer, pressure and gyro meter micro sensors.

Wireless Remote Power Sensing (WRPS) is basically the association of two functions: a tag circuitry and a micro-sensor with its interface. This contactless micro-system is a key element of the trumpeted "ambient intelligence". Portable readers built around a mobile phone will activate these information nodes (see figure 19).

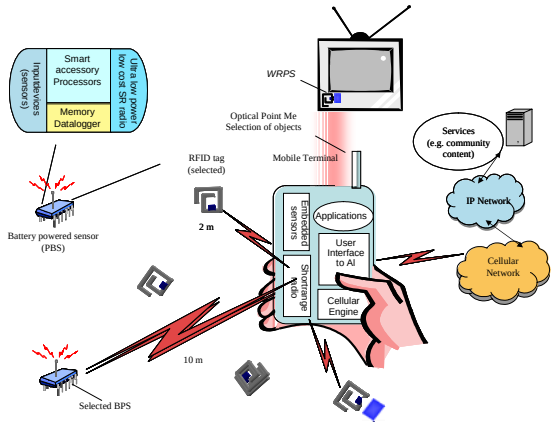


Fig. 19: Typical scenario of ambient intelligence

Another application area of contactless sensors is in vivo medical monitoring. On the next figure, an intra lung pressure measurement micro system is shown. This microsystem is introduced at the end of a catheter of 1.5 mm of diameter with a miniaturized antenna and placed into the body of the patient. An antenna is placed on the thorax of the patient and connected to the reader. Continuous monitoring of in vivo parameters is performed without the drawback of wiring and lithium battery inside the body of the patient.

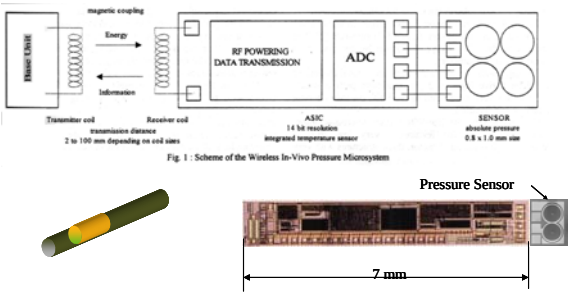


Fig. 20: Contactless microsystem for in vivo pressure measurement

9. Conclusions

This paper has shown several new technological avenues that are currently under development in R&D laboratories. Today two main evolutions of RFID chip are foreseen: the integration of micro-sensors for data logging and the increase in processing capabilities (higher data rates and cryptography) versus power requirements to tackle the security aspect.

References:

[1] P. Villard et al. , "The Benefit of SOI Technology for Low-Voltage RFID applications", ECS 03

[2] H. Rouault et al. , "PEA Card or Power Embedded Active Card", e-Smart 04

[3] E. Crochon et al. , "New Emerging Technologies for Contactless Air Interfaces". E-Smart 05

[4] D. Caucheteux, "Transmissions asynchrones à débit dynamiquement variable pour étiquettes sans contact et téléalimentés". TAISA 05

[5] S. Bacquet et al., "PEACPocket: a technological demonstrator for future multimedia smart card". sOc-EuSAI 05